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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,338	02/22/2002	Jia-Fam Wong	B-4506 619547-1	9829

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EXAMINER

DI GRAZIO, JEANNE A

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/081,338

Applicant(s)

WONG, JIA-FAM

Examiner

Jeanne A. Di Grazio

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Priority*

Priority to Taiwan Patent Application No. 90107642 (March 30, 2001) is claimed.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 7, 10, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 145) in view of Kurauchi et al. (US '921 B1).

Per claims 1 and 7: Suzuki has the steps of forming a wiring pattern for a multi layer wiring structure on a substrate, forming a first insulating layer over the wiring pattern, forming a second insulating layer over a wiring layer, and forming a third insulating layer over a wiring layer (See Figure 5D). Suzuki has pixel areas covered by the multiple insulating layers. In Suzuki, the insulating layers are etched (Col. 6, Lines 21-37) such that the insulating layers substantially function as resist layers. Suzuki furthermore has the structure defined by the method (Figure 5D). Suzuki does not appear to have the step of forming a plurality of signal lines and a plurality of gate lines that cross each other and the step of forming a switching unit in each pixel area; however, Kurauchi teaches that a matrix substrate generally includes plural scanning lines and plural signal lines intersecting with each other, switching elements (thin film transistors) at the intersecting regions, and pixel electrodes (Col. 6, Lines 34-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify

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Suzuki in view of Kurauchi to form an active matrix display and for switching the active matrix display.

Per claims 4, 10, and 16: Suzuki discloses the optional method of forming a protective film or the like between a lower-layer wiring pattern and first insulating film (Col. 15, Lines 54-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a passivation layer between switching units and first photoresist layer for preventing contact between the switching units and first photoresist layer (Id.).

Per claim 13: Suzuki has the steps of forming a wiring pattern for a multi layer wiring structure on a substrate, forming a first insulating layer over the wiring pattern, forming a second insulating layer over a wiring layer, and forming a third insulating layer over a wiring layer (See Figure 5D). Suzuki has pixel areas covered by the multiple insulating layers. In Suzuki, the insulating layers are etched (Col. 6, Lines 21-37) such that the insulating layers substantially function as resist layers. Suzuki furthermore has the structure defined by the method (Figure 5D). Suzuki does not appear to have the step of forming a plurality of signal lines and a plurality of gate lines that cross each other and the step of forming a switching unit in each pixel area; however, Kurauchi teaches that a matrix substrate generally includes plural scanning lines and plural signal lines intersecting with each other, switching elements (thin film transistors) at the intersecting regions, and pixel electrodes (Col. 6, Lines 34-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki in view of Kurauchi to form an active matrix display and for switching the active matrix display. First and second substrates with liquid crystal in between the substrates is common in the art (See, e.g., Kurauchi at Col. 1, Lines 14-16).

Claims 2, 3, 5, 6, 8, 9, 11, 14, 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 145) and Kurauchi et al. (US '921 B1) in further view of Lin et al. (US '653).

Per claims 2, 8, and 14: Suzuki does not appear to address TFTs as switching units; however, Kurauchi does have TFTs as noted (Col. 6, Lines 34-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki in view of Kurauchi because TFTs are commonly used as switching devices. Suzuki, as can be seen in at least Figure 5D, illustrates at least a through hole that pierces through three insulating layers and the at least through hole exposes a section of a wiring pattern (62) as can also be seen in Figure 5D. Suzuki does not appear to specify that the drain electrode is exposed; however, Lin uses a back-etch method to expose drain electrodes through photoresist layers [See, ABS]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki in view of Lin to facilitate connections through multiple layers and to reduce the number of necessary connections.

Per claims 3, 6, 9, 12, 15, and 18: Suzuki discloses the depositing of a conductive material to cover the insulating films (Col. 14, Lines 60-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a conductive layer to fill in connecting holes and to cover the insulating layers (Col. 14, Lines 60-64).

Per claims 5, 11, and 17: Because Suzuki discloses that a protective film may be formed between the lower-layer wiring pattern and first insulating film, and a through hole pierces through the three insulating layers as shown in Figure 5D, the through hole may also pierce

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through the protective film if so desired to facilitate connections to the wiring layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki in view of Lin to include a through hole through the photoresist layers and passivation film to facilitate connection to the wiring patterns.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (703)305-7009. The examiner can normally be reached on M-F.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (703) 305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-8741 for regular communications and (703)746-8741 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jeanne Andrea Di Grazio

JDG  
April 14, 2003

~~Robert Kim, SPE~~

  
T. Chowdhury  
Primary Examiner